IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the Application of: **HASHIMOTO, Hiroshi et al.**

Serial No.: **09/960,399**

Group Art Unit: **2814**

Filed: **September 24, 2001**

Examiner: **Howard Weiss**

P.T.O. Confirmation No.: 5652

For. **A SEMICONDUCTOR INTEGRATED CIRCUIT AND FABRICATION PROCESS HAVING COMPENSATED STRUCTURES TO REDUCE MANUFACTURING DEFECTS (as amended)**

#8/Drwgs.
Martha
10/8/02

REQUEST FOR APPROVAL OF DRAWING CHANGES

Commissioner for Patents
Washington, D.C. 20231

October 1, 2002

Sir:

The Examiner's approval of the drawing corrections indicated in red ink on the attached 51 sheets of drawings is respectfully requested.

Upon receipt of approval of the drawing corrections and a formal Notice of Allowance, a bonded draftsman will be retained and the appropriate corrections will be made.

In the event any fees are required in connection with this paper, please charge our Deposit Account No. 01-2340.

Respectfully submitted,
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GNS/alw
Atty. Docket No. **011225**
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Attachment: 51 Sheets of Corrected Drawings